IN THE SPECIFICATION:

Please amend the specification by inserting the following new paragraph immediately before line 1 of page 1:

--This is a Divisional of copending U.S. Application No. 09/625,643, filed on July 25, 2000.--

Please substitute the paragraph starting on page 6, line 13 with the following paragraph:

--Further, as can be seen in Fig. 10B, for [~~For~~] communicating signals between the internal circuits 4A, 4B, inter-circuit signal wires 12 for interconnecting the output element 12A of the internal circuit 4A and the input [~~output~~] element 12B of the internal circuit 4B, and inter-circuit signal wires 13 for interconnecting the output element 13B of the internal circuit 4B and the input element 13A of the internal circuit 4A are also routed between the internal circuits 4A, 4B as many number of lines as required for communicating signals.--

Please substitute the paragraph starting on page 6, line 21 with the following paragraph:

--The output element 12A may comprise a single or a plurality of active elements such as transistors. For example, if the output element 12A is a CMOS inverter (see Fig. 11A), the output element 12A includes a p-type MOS (hereinafter called the "pMOS") transistor 12AP having a source connected to the power line 8A, a drain connected to the inter-circuit signal wire 12, and a gate connected to an internal signal wire SA within the internal circuit 4A; and an n-type MOS (hereinafter called the "nMOS") transistor 12AN having a source connected to the

power line 9A, a drain connected to the inter-circuit signal wire 12, and a gate connected to the internal signal wire SA within the internal circuit 4A. The input element 12B also includes a pair of transistors, pMOS transistor 12BP and nMOS transistor 12BN, having their sources connected to the power lines 8B, 9B, respectively, which have their gates connected to the inter-circuit signal wire 12, and their drains connected to an internal signal wire SB within the internal circuit 4B.--

Please substitute the paragraph starting on page 7, line 11 with the following paragraph:

--The input element 13A and the output element 13B, though signals are communicated in directions opposite to each other, each includes [~~include~~] a similar transistor pair consisting of one pMOS transistor (13AP, 13BP [~~13AN~~]) and one nMOS transistor [pair] (13AN [~~13BP~~], 13BN), with their drains or gates connected to the inter-circuit signal wire 13.--

Please substitute the paragraph starting on page 9, line 11, with the following paragraph:

--Specifically, as can be seen in Fig. 11D, basic cells of interest are formed with contact holes (see a black line [~~circuit~~] in Fig. 11D) such as via holes at the centers thereof to connect the sources of the active elements 12AP, 12AN, 12BP, 12BN in the first connection configuration to the power lines 8A, 9A, 8B, 9B, respectively. In the internal circuit 4A, the internal signal wire SA is connected to the gate of the active element 12AP in the first connection configuration as well as to the gates of both the active elements 12AP, 12AN in the first connection configuration. Also, one end of the inter-circuit signal wire 12 is branched and connected to the drains of the active elements 12AP, 12AN in the first configuration at corners of the basic cells.--

Please substitute the paragraph starting on page 12, line 6, please substitute the following paragraph:

--Also, in such a situation, if surge noise is introduced, for example, into the input/output terminal 7B (see Fig. 12C), the existence of the input protection circuit 3B for protecting the internal element 11B may adversely affect the other internal element 12B and so on. The surge noise will be forced to escape to the power lines 8B, 9B through the input protection circuit 3BB, and then is discharged to the outside from the lower power terminal 5B and the ground terminal 6B, and also propagates and diffuses across the internal circuit 4B. In this event (see two-dot chain lines and so on in Fig. 12C), the difference between a time required for the surge noise to reach the active element 12BP in the first connection configuration through the power line 8B and a time required for the surge noise to reach the active element 12BN in the first connection configuration through the power line 9B cannot be ignored. In addition, it is also contemplated that an element which has been intensively and locally affected by the difference in potential with the inter-circuit signal wire 12 has also become more susceptible to failure.--

Please substitute the paragraph starting on page 14, line 5 with the following paragraph:

--A semiconductor integrated circuit device according to a first aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 1 to 4,~~] a semiconductor integrated circuit device which has (in a single chip) a plurality of internal circuits having different [~~difference~~] power lines (for a positive voltage, a negative voltage, a higher voltage, a lower voltage, a ground, and so on), and an inter-circuit signal wire arranged to interconnect these (at least any one pair of) internal circuits (for

communicating signals between the internal circuits), wherein near an active element in a first connection configuration (for inputting a signal or for outputting a signal) connected to the inter-circuit signal wire, a plurality of active elements in another connection configuration are arranged to (directly or indirectly) sandwich or surround the active element in the first connection configuration. The active elements in the other connection configuration include elements of an identical or similar structure to the active element in the first connection configuration in repetitions (of the same types or in a mixture of different types), and are connected to power lines of the internal circuits associated therewith and isolated from signal wires other than the inter-circuit signal wire (specifically, any of active elements in a second, a third, a fourth connection configuration, or protection elements like these which are connected to power lines of the internal circuits associated therewith but not connected to signal wires in the internal circuit).--

Please substitute the paragraph starting on page 15, line 3 with the following paragraph:

--In the semiconductor integrated circuit according to the first aspect of the present invention [~~solution~~] as described above, in a normal state without surge noise or the like, the newly introduced active elements in the other connection configuration are not connected to signal wires in the internal circuit, so that the active elements in the other connection configuration will not prevent proper operations of the active element in the first connection configuration or other internal elements. On the other hand, if surge noise is introduced into an external connection terminal and propagates through power lines, and reaches the active element in the first connection configuration at different times through the respective power lines, a portion of the surge noise is immediately led from the power line through which the noise had reached earlier to the power line through which the noise has reached later through the active

elements in the other connection configuration. This operation is performed at a plurality of locations on both sides of or around the active element in the first connection configuration.--

Please substitute the paragraph starting on page 17, line 1 with the following paragraph:

--A semiconductor integrated circuit device according to a second aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 5 to 9,~~] a semiconductor integrated circuit device which has (in a single chip) a plurality of internal circuits having difference power lines (for a positive voltage, a negative voltage, a higher voltage, a lower voltage, a ground, and so on), and an inter-circuit signal wire arranged to interconnect these (at least any one pair of) internal circuits (for communicating signals between the internal circuits), wherein near an active element in a first connection configuration (for inputting a signal or for outputting a signal) connected to the inter-circuit signal wire, an active element in a second connection configuration of an identical or similar structure to the active element in the first connection configuration (for protection which is not connected directly to any signal wires driven by active elements other than itself) is arranged and connected to power lines of the internal circuits associated therewith and isolated from the inter-circuit signal wire and other signal wires.--

Please substitute the paragraph starting on page 17, line 19 with the following paragraph:

--In the semiconductor integrated circuit according to the second aspect of the present invention [~~solution~~] as described above, the newly introduced active element in the second connection configuration is not connected to signal wires in the internal circuit or to the inter-circuit signal wire, as is the case of the active element in the other connection configuration, so that the active element in the second connection configuration will not prevent proper operations

of the active element in the first connection configuration and so on in a normal state. On the other hand, if in an abnormal state in which entering surge propagates through power lines, and reaches the active element in the first connection configuration at different times through the respective power lines, a portion of the surge noise is immediately led from the power line through which the noise had reached earlier to the power line through which the noise has reached later. In this way, fluctuations in potential due to the surge noise are dispersed near the active element in the first connection configuration to suppress its peak to a low level. Further, as to locations for sharing the influence of the inter-circuit signal wire, the influence is dispersed to locations at which the respective power lines are connected, thus further suppressing the peak of potential difference to a low level.--

Please substitute the paragraph starting on page 19, line 4 with the following paragraph:

--A semiconductor integrated circuit device according to a third aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 10 to 14,~~] the semiconductor integrated circuit device according to the second aspect of the present invention [~~solution~~] which further comprises an active element in a third connection configuration (for protection which is not connected directly to any of signal wires driven by active elements other than itself except for the inter-circuit signal wire), arranged near the active element in the first connection configuration and including an element of an identical or similar structure to the active element in the first connection configuration, wherein the active element in the third connection configuration is connected to power lines of an internal circuit associated therewith and the inter-circuit signal wire, and isolated from other signal lines.--

Please substitute the paragraph starting on page 19, line 18 with the following paragraph:

--In the semiconductor integrated circuit device according to the third aspect of the present invention [~~solution~~] as described above, the active element in the third connection configuration, though connected to the inter-circuit signal wire, is introduced only in regions where the active element is unlikely to prevent signal transmission in a normal state, in additional consideration to the magnitude of supply voltage. In regions where the active element in the third connection configuration is likely to prevent signal transmission in a normal state, the active element in the second connection configuration is provided instead. Then, for surge noise as mentioned above, in addition to the aforementioned protection provided by the active element in the second connection configuration, the active element in the third connection configuration more positively disperses the influence of the inter-circuit signal wire, though depending on the direction of the noise, to further suppress the peak of the potential different to a lower level. In addition, the active element in the third connection configuration newly introduced as a protection element is also implemented in a similar procedure to those of the aforementioned active elements in the first and second connection configurations.--

Please substitute the paragraph starting on page 20, line 16 with the following paragraph:

--A semiconductor integrated circuit device according to a fourth aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 15 to 19,~~] the semiconductor integrated circuit device according to the third aspect of the present invention [~~solution~~], wherein a plurality of the inter-circuit signal wires having different communication directions from each other are arranged in (at least) any one pair of the plurality of internal circuits, the active element in the second connection configuration and the active element in the third connection configuration are arranged near the active element in the

first connection configuration on a reception side (i.e., for inputting signals) of the inter-circuit signal wire in one of the pair of internal circuits (i.e., an internal circuit which is fed with a relatively lower supply voltage), and (preferably, a plurality of) the active elements in the third connection configuration are arranged instead of or exclusive of the active element in the second connection configuration (i.e, without providing the active element in the second connection configuration), near the active element in the first connection configuration on a reception the (i.e., for inputting signals) of the inter-circuit signal wire in the other of the pair of internal circuits (i.e., an internal circuit which is fed with a relatively higher supply voltage).--

Please substitute the paragraph starting on page 21, line 11 with the following paragraph:

--In the semiconductor integrated circuit device according to the fourth aspect of the present invention [~~solution~~] as described above, the active elements in the second and third connection configurations are provided in combination as appropriate in a region which is restricted in connectivity to an active element to both the inter-circuit signal wire and the power line due to the possibility of the voltage on the inter-circuit signal wire exceeding the voltage on the power line at that location depending on the value of a signal on the inter-circuit signal wire (such a region is typically a reception side of the inter-circuit signal wire in an internal circuit fed with the relatively lower supply voltage, i.e., an input element), and the active element in the third connection configuration is provided at least one and as many as possible in a region which is free of such restriction and is vulnerable to the influence of the inter-circuit signal wire (such a region is typically a reception side of the inter-circuit signal wire in an internal circuit fed with the relatively higher supply voltage, i.e., an input element).--

Please substitute the paragraph starting on page 22, line 12 with the following paragraph:

--A semiconductor integrated circuit device according to a fifth aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 20 to 23,~~] a semiconductor integrated circuit device which comprises (in a single chip) a plurality of internal circuits having different power lines (for a positive voltage, a negative voltage, a higher voltage, a lower voltage, a ground, and so on), and an inter-circuit signal wire arranged to interconnect these (at least any one pair of) internal circuits (for communicating signals between the internal circuits), wherein an inter-circuit auxiliary wire (preferably, running in parallel with the inter-circuit signal wire) is connected to a static area (i.e., an area where an electrical condition does not dynamically change in a normally operating state such as a location to which any signal wire is not directly connected) near a location at which the inter-circuit signal wire is connected.--

Please substitute the paragraph starting on page 23, line 1 with the following paragraph:

--In the semiconductor integrated circuit device according to the fifth aspect of the present invention [~~solution~~] as described above, while the inter-circuit auxiliary wire is newly introduced, this wire is [~~not~~] connected to a location at which an electrical condition does not dynamically change in a normally operating state free of surge noise or the like, so that the inter-circuit auxiliary wire will not prevent proper operations of the active element in the first connection configuration and other internal elements. On the other hand, if surge noise is introduced into any external connection terminal and propagates only to one internal circuit to cause an increased potential difference with the other internal circuit to result in a sudden change in the potential locally at an active element in the first connection configuration in the one internal circuit connected to the other internal circuit through the inter-circuit signal wire, the

existence of the inter-circuit auxiliary wire will give rise to a similar potential change at a point near the active element in the first connection configuration. Subsequently, if the potential change propagates to the active element in the first connection configuration, the potential of the entire active element in the first connection configuration will also move to some degree toward the sudden potential at the location at which the inter-circuit signal wire is connected, so that the potential difference between a location connected to the inter-circuit signal wire and a location not connected to the inter-circuit signal wire is canceled by that portion in the active element in the first connection configuration.--

Please substitute the paragraph starting on page 24, line 18 with the following paragraph:

--A semiconductor integrated circuit device according to a sixth aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 24 to 28,~~] the semiconductor integrated circuit device according to the fifth aspect of the present invention [~~solution~~], wherein the static area (several static areas connected to the inter-circuit auxiliary wire) includes a partial region of an active element on a transmission side of the active elements in the first connection configuration (i.e., for outputting signals) connected to the inter-circuit signal wire, which partial region is connected to a power line of the internal circuit associated therewith, and an active element (i.e., an active element in a fourth connection configuration for protection which is not directly connected to any of signal wires driven by active elements other than itself) in another connection configuration having an identical or similar structure to the active element in the first connection configuration on a reception side (i.e., for inputting signals), arranged near the active element in the first connection configuration, and isolated from signal wires other than the inter-circuit auxiliary wire (except for a connection to the power line).--

Please substitute the paragraph starting on page 25, line 11 with the following paragraph:

--In the semiconductor integrated circuit device according to the sixth aspect of the present invention [~~solution~~] as described above, the active element in the fourth connection configuration (the active element in the other connection configuration), though connected to the internal-circuit auxiliary wire, is only introduced in a region where a different power supply is not short-circuited in a normal state, in additional consideration to the magnitude of supply voltage. With the provision of the active element in the fourth connection configuration, local potential fluctuations produced in an active element in the first connection configuration located near the active element in the fourth connection configuration are not only followed by similar potential fluctuations due to the inter-circuit auxiliary wire but also forced to positively escape through the active element in the fourth connection configuration and the inter-circuit auxiliary wire.--

Please substitute the paragraph starting on page 26, line 13 with the following paragraph:

--A semiconductor integrated circuit device according to a seventh aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claim 29,~~] the semiconductor integrated circuit device according to the sixth aspect of the present invention [~~solution~~], wherein the inter-circuit auxiliary wire is connected to a neighboring region overlapping with or close to the partial region on the power line connected thereto, instead of the partial region. --

Please substitute the paragraph starting on page 26, line 20 with the following paragraph:

--In the semiconductor integrated circuit device according to the seventh aspect of the present invention [~~solution~~] as described above, the inter-circuit auxiliary wire is connected to a different location which is equivalent in function because of its closeness to the partial region. This results in an increased width of selection during the design of wiring, and relieved restrictions, so that the designing becomes easier. It is therefore possible, according to this invention, to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and more suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 27, line 4 with the following paragraph:

--A semiconductor integrated circuit device according to an eighth aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 30 - 34 and claims 35 - 39,~~] the semiconductor integrated circuit device according to the sixth or seventh aspects of the present invention [~~solution~~], wherein a plurality of the inter-circuit signal wires having different communication directions from each other are arranged in (at least) any one pair of the plurality of internal circuit, an active element in a further connection configuration (i.e., the active element in the second connection configuration which is not directly connected to any of signal wires driven by active elements other than itself) having an identical or similar structure to the active element in the other connection configuration is arranged in addition to the active element in the other connection configuration (i.e., the active element in the fourth connection configuration) near an active element in the first connection configuration on a reception side (i.e., for inputting signals) of the inter-circuit signal wire in one of the pair of internal circuits (i.e., an internal circuit fed with a relatively lower supply voltage), wherein the active element in the further connection configuration connected to a power line of

the internal circuit and isolated from the inter-circuit signal wire, other signal wires and the inter-circuit auxiliary wire, and (preferably, a plurality of) the active elements in the other connection configuration (i.e., the active element in the fourth connection configuration) are arranged instead of or exclusive of the active element in the further connection configuration (i.e., the active element in the second connection configuration) (i.e., without providing the active element in the second connection configuration), near the active element in the first connection configuration on a reception side (i.e., for inputting signals) of the inter-circuit signal wire in the other of the pair of internal circuits (i.e., an internal circuit fed with a relatively higher supply voltage).--

Please substitute the paragraph starting on page 28, line 10 with the following paragraph:

--In the semiconductor integrated circuit device according to the eighth aspect of the present invention [~~solution~~], the active elements in the fourth connection configuration (the active element in the other connection configuration) and the active element in the second connection configuration (the active element in the further connection configuration) are provided in combination as appropriate in a region which is restricted in connectivity to an active element to both the inter-circuit signal wire and the power line and is vulnerable to the influence of the inter-circuit signal wire (such a region is typically a reception side of the inter-circuit signal wire in an internal circuit fed with the relatively lower supply voltage, i.e., an input element), and the active element in the fourth connection configuration is provided as many as possible in a region which is free of such restriction and is vulnerable to the influence of the inter-circuit signal wire (such a region is typically reception side of the inter-circuit signal wire in an internal circuit fed with the relatively higher supply voltage, i.e., an input element).--

Please substitute the paragraph starting on page 29, line 11 with the following paragraph:

--A semiconductor integrated circuit device according to a ninth s aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 6, 11, 16, 25, 31, 36,~~] the semiconductor integrated circuit device according to the second to eighth aspects of the present invention [~~solutions~~], wherein a plurality of the active elements in the second, third, other, and further connection configurations or those corresponding thereto (i.e., protection elements arranged near the active element in the first connection configuration, and connected to a power line of the internal circuit associated therewith but not connected to signal wires in the internal circuit) are arranged to (directly or indirectly) sandwich or surround the active element in the first connection configuration (in repetitions of the same type or in mixture of different types). --

Please substitute the paragraph starting on page 29, line 24 with the following paragraph:

--In the semiconductor integrated circuit device according to the ninth aspect of the present invention [~~solution~~]as described above, surge noise is bypassed or dispersed at a plurality of locations such as on both sides or around the active element in the first connection configuration, so that the surge noise is substantially uniformly mitigated to keep the balance at a plurality of points or multiple points.--

Please substitute the paragraph starting on page 30, line 13 with the following paragraph:

--A semiconductor integrated circuit device according to a tenth aspect of the present invention [~~solution~~]invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 40 - 43,~~] a semiconductor integrated circuit device, wherein, for a signal wire which originates from an external connection terminal, passes through an input/output circuit in one of

a plurality of sets comprised of any of the internal circuits and any of the input/output circuits, connected to different power lines, and reaches the internal circuit included in the same set as the input/output circuit, a first protection circuit is provided in the input/output circuit of the one set for the signal wire to protect the internal circuit of the one set from electrostatic breakdown, and additionally, for a branched wire which is branched from the signal wire and reaches an internal circuit in any of the plurality of sets, a second protection circuit is provided in the input/output circuit in the other set after the branched wire is passed through the input/output circuit of the other set before it reaches the internal circuit of the same set, and a third protection circuit is also provided in the internal circuit in the other set for the branched wire, so that the internal circuit in the other set can be protected from electrostatic breakdown at multiple stages.--

Please substitute the paragraph starting on page 31, line 8 with the following paragraph:

--A semiconductor integrated circuit device according to an eleventh aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claim 44,~~] the semiconductor integrated circuit device according to the tenth aspect of the present invention [~~solution~~], wherein in a region where it is difficult to directly connect a portion or all of protection elements included in the first, second and third protection circuits to the signal wire or the branched wire due to a difference in supply voltage or the like, an active element is connected to a power line of an associated input/output circuit or an associated internal circuit, and isolated from any signal wire such that the active element acts as a protection element.--

Please substitute the paragraph starting on page 31, line 19 with the following paragraph:

--A semiconductor integrated circuit device according to a twelfth aspect of the present invention [~~solution~~] invented to solve the problem mentioned above is[~~, as set forth in originally filed claims 43 and 45,~~] the semiconductor integrated circuit device according to the tenth or eleventh aspects of the present invention [~~solution~~], wherein the third protection circuit includes a plurality of protection elements which are arranged to sandwich or surround an element to be protected, thereby protecting the element from the surroundings.--

Please substitute the paragraph starting on page 34, line 20 with the following paragraph:

--Figs. 12A-12C illustrate adverse influences [Fig. 12 is an imaginary diagram illustrating the influence] of surge noise [related to the presentation of the problem].--

Please substitute the paragraph starting on page 42, line 1 with the following paragraph:

--With the modified configuration set forth above, the pMOS transistors 25, 27 remain as active elements in the second connection configuration for protecting the active element 12BP in the first connection configuration from both left and right sides, whereas the nMOS transistors 26, 28 are positioned near the active element 12BN in the first connection configuration so as to sandwich the active element 12BN on both left and right sides. While the nMOS transistors 26, 28 are of the same n-type as the associated active element 12BN in the first connection configuration and are connected to the power line [~~lines 8B,~~] 9B in the internal circuit 4B and the inter-circuit signal wire 12, the nMOS transistors 26, 28 are not connected to other signal wires so that they function as active elements in a third connection configuration for protecting the active element 12BN in the first connection configuration from the surroundings.--

Please substitute the paragraph starting on page 47, line 18 with the following paragraph:

--With the introduction of the inter-circuit auxiliary wire 29, nMOS transistors 26, 28 have their drains connected to the inter-circuit auxiliary wire 29 instead of the inter-circuit signal wire 12. Specifically, the inter-circuit auxiliary wire 29 has the other end connected to the transistors 26, 28 in the internal circuit 4B. With such connections, the transistors 26, 28 act as active elements in a fourth connection configuration having the identical or similar structure to the active element 12BN in a first connection configuration on the reception side of signal transmission [~~transmition~~], are positioned near the active element 12BN, and are isolated from signal wires other than the inter-circuit auxiliary wire 29. It can therefore be said that these are also static areas.--

Please substitute the paragraph starting on page 48, line 11 with the following paragraph:

--In this circuit configuration, any of the inter-circuit auxiliary wire 29 and the nMOS transistors 26, 28 is not connected to signal wires in the internal circuits 4A, 4B, and the nMOS transistors 26, 28 will not become conductive as long as the voltage on the power line 8A and the voltage on the power line 9A are not inverted or excessively separated, so that the introduction of the inter-circuit auxiliary wire 29 will not damage proper operations of the internal circuits 4A, 4B. In addition, since the nMOS transistors 26, 28 and so on are isolated from the inter-circuit signal wire 12, signals on the inter-circuit signal wire 12 will not be delayed or reduced, the semiconductor integrated circuit device of the fourth embodiment provides preferred performance, and moreover can be readily applied even to applications which require fast operations.--

Please substitute the paragraph starting on page 50, line 23 with the following paragraph:

--The semiconductor integrated circuit device of the fifth embodiment differs from the fourth embodiment illustrated in Figs. 4A and 4B in that the inter-circuit auxiliary wire 29 has its end near the output [~~input~~] element 12A [~~12B~~] connected to the power line 8A instead of the source of the active element 12AP in the first connection configuration.--

Please substitute the paragraph starting on page 56, line 26 with the following paragraph:

--Similarly, for a signal wire 44B, a first protection circuit 3XB is provided in the input/output circuit 3B, and a branched wire 45A branched from the protection circuit 3XB extends separately from the set of the input/output circuit 3B and the internal circuit 4B. The branched wire 45A passes through the input/output circuit 3A in the other set, reaches the internal circuit 4A in the same set, and is connected to an input element 42A. For this branched wire 45A[[~~45~~]], a second protection circuit 43A is provided in the input/output circuit 3A, and third protection circuit comprising components 63 - 66 is provided near the input element 42A in the internal circuit 4A.--

Please substitute the paragraph starting on page 66, line 10 with the following paragraph:

--As will be apparent from the foregoing descriptions, a semiconductor integrated circuit device according to a first aspect of the invention [~~solution~~] of the present invention promptly and uniformly disperses fluctuations in potentials due to surge noise near an active element in the first connection configuration to suppress the peak of the fluctuations, and newly introduced protection elements are implemented in a procedure similar to that of the active elements in the first connection configuration, and so on, thereby making it possible to realize a semiconductor

integrated circuit device which is resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 66, line 21 with the following paragraph:

--Also, a semiconductor integrated circuit device according to a second aspect of the invention [~~solution~~] of the present invention promptly disperses fluctuations in potential due to surge noise near an active element in the first connection configuration to suppress the peak of the fluctuations, and newly introduced protection elements in the second connection configuration are implemented in a procedure similar to that of the active elements in the first connection configuration, and so on, and moreover act as protection elements irrespective of the magnitude of supply voltage, thereby making it possible to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 67, line 7 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a third aspect of the invention [~~solution~~] of the present invention introduces active elements in a third connection configuration which positively disperse the influence of an inter-circuit signal wire and which is implemented in a procedure similar to those of the active elements in the first and second connection configurations, thereby making it possible to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 67, line 17 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a fourth aspect of the invention [~~solution~~] of the present invention employs many active elements in the third connection configuration positioned on a reception side of an internal circuit, which is more vulnerable to the influence on an inter-circuit signal wire, for positively distributing the influence of the inter-circuit signal wire, thereby making it possible to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 67, line 25 with the following paragraph:

--Further, in a semiconductor integrated circuit device according to a fifth aspect of the invention [~~solution~~] of the present invention, local potential fluctuations caused by the inter-circuit signal wire and the inter-circuit auxiliary wire are superimposed to suppress the peak of potential differences generated in the active elements in the first connection configuration, and the new protection circuits can be introduced by additionally changing associated wiring patterns, thereby making it possible to realize a semiconductor integrated circuit device which is resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 68, line 9 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a sixth aspect of the invention [~~solution~~] of the present invention disperses the influence of the inter-circuit signal wire exerted to the reception side, which is relatively vulnerable, toward the transmission side, which is relatively strong, thereby making it possible to realize a semiconductor integrated

circuit device which is more resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 68, line 17 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a seventh aspect of the invention [~~solution~~] relieves restrictions related to a location at which the inter-circuit auxiliary wire is connected, thereby making it possible to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and more suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 68, line 23 with the following paragraph:

--Further, a semiconductor integrated circuit device according to an eighth aspect of the invention [~~solution~~] uses many active elements in the fourth connection configuration around the reception side, which is vulnerable to the influence of the inter-circuit signal wire, for positively distributing the influence of the inter-circuit signal line, thereby making it possible to realize a semiconductor integrated circuit device which is more resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 69, line 5 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a ninth aspect of the invention [~~solution~~] promptly and uniformly disperses potential fluctuations due to surge noise near active elements in the first connection configuration to limit the peak of the fluctuations, so that enhanced protection can be provided for the active elements in the first connection

configuration, thereby making it possible to realize a semiconductor integrated circuit device which is resistant to electrostatic breakdown and suitable to automatic designing and so on.--

Please substitute the paragraph starting on page 69, line 14 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a tenth aspect of the invention [~~solution~~] protects internal circuits, to which branched wires are routed, in the internal circuits themselves as well as in input/output circuits in the midway, to multiply explicit and direct protection in addition to supplementary protection in input/output circuits in another power system, thereby making it possible to enhance the protection of the internal circuits from electrostatic breakdown.--

Please substitute the paragraph starting on page 69, line 22 with the following paragraph:

--Further, a semiconductor integrated circuit device according to an eleventh aspect of the invention [~~solution~~] can protect internal circuits even without direct connections to signal wires or branched wires, to ensure that a protection circuit can be provided even for an internal circuit connected to a circuit in another power system through a signal wire or a branched wire.--

Please substitute the paragraph starting on page 70, line 2 with the following paragraph:

--Further, a semiconductor integrated circuit device according to a twelfth aspect of the invention [~~solution~~]protects an element of interest from the surroundings, so that local fluctuations in potential difference around the element of interest, if any, will be dispersed to the surroundings to promptly limit the peak of the potential difference, thereby making it possible to further enhance the protection of internal circuits from electrostatic breakdown.--